Porous Ultra Low-k Material Integration Through An Extended Dual Damascene Approach: Pre-/ Post-CMP Curing Comparison

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Abstract

Integration of dielectrics with increased porosity is required to reduce the capacitance of interconnects. However, the conventional dual damascene integration approach is causing negative effects to these materials avoiding their immediate implementation. A post-CMP curing approach could solve some of these issues. However, materials with porogens being stable at temperatures of the barrier-seed deposition process are not common, hindering this approach. Here, we report on an extended dual-damascene integration approach which permits post-CMP curing.

1. Introduction

Integration of porous ultra low-k (ULK) materials is required to reduce resistive-capacitive (RC) delay, power consumption and cross-talk noise of back-end-of-line (BEOL) interconnects [1].

However, the integration of ULK materials faces many issues with conventional dual damascene approaches, since all processes are executed after the porous dielectric is cured. The dielectric is exposed to plasma induced damage from reactive ion etching and stripping chemistries, to wet cleaning with consequent water absorption, to metal intrusion from the barrier-seed deposition and to damage related to the CMP. Furthermore, the liner integrity will become challenging with increasing pore sizes [2].

To reduce these drawbacks, other integration approaches have to be developed. Post chemical mechanical polishing (CMP) curing or post-CMP burn-out (PCBO) have been developed to keep the porosity until later stages (porosity last approach). However, materials with porogens being stable at temperatures of the barrier-seed deposition process (~350 °C) are not common. So the dielectric starts decomposing during these processes [3].

Hence, an alternative porous integration approach based on a sacrificial dielectric is presented. The sacrificial dielectric can be removed by either wet etching or reactive ion etching [4,5]. Here, we use the reactive ion etching anisotropic removal of the sacrificial dielectric. Afterwards, a porous ULK is deposited. Therefore, any porous ULK can be used since the structures are already patterned. This opens the possibility to integrate a much larger variety of porous materials (e.g. mesoporous materials deposited by spin-on). With this alternative ULK integration approach, the dielectric curing can be the last process before deposition of the dielectric diffusion barrier. This study compares two CMP scenarios of the alternative ULK integration with cure either done pre or post CMP (Figure 1). Parameters investigated after CMP were ULK roughness, porosity and CMP removal rates.

2. Experimental

28 nm technology node structures were patterned on 300 mm wafers by a conventional dual damascene flow. A selective CoWP cap was deposited after CMP by electroless deposition to protect the Cu structures during reactive ion etching. The original dielectric, used as sacrificial layer, was anisotropically etched by reactive ion etching on an AMAT Centura platform. A SOL-GEL material was used to replace the original dielectric. The deposition was done on a Brewer Science 100 FX spin coater and soft baked at 150 °C on a 100 FX Hotplate from Brewer Science. A CMP process was developed for the planarization of the spin-on dielectric using an AMAT Reflexion LK with silica amorphous slurry, a soft conformal pad and tetra-methyl ammonium hydroxide (TMAH) based post-CMP clean.

The spin-on dielectric was cured on a TEL formula annealer under vacuum with nitrogen for 2 hours at 400 °C. The SOL-GEL was transformed by the cure process into an organo silicate glass (OSG) with a k-value of 2.5. The integration approach is shown in Figure 1. The film thicknesses and refractive indexes were measured by ellipsometry on a KLA Spectra FX-100. The surface roughness was measured by an X3D 3-D Atomic Force Microscope (AFM) from Veeco. Open porosity was determined by an ellipsometric porosimeter (EP) from Sopralab using toluene as solvent. For thickness determination on patterned wafers, a HRP340 Planarity Metrology Tool from KLA Tencor was used. Scanning

electron microscope (SEM) in combination with a Focused Ion Beam (FIB) provided cross-section pictures.

3. Results and Discussion

3.1 Roughness measurements

The interface between ultra low-k dielectric and dielectric diffusion barrier (ULK/ SiCN) is very critical for time-dependent dielectric breakdown (TDDB) [6]. If a thinner diffusion barrier layer can be deposited, the effective k-value of the final interconnects will be lower. The ULK roughness has to be as low as possible in order to use thinner dielectric caps with sufficient barrier properties. AFM measurements were carried out in order to measure the roughness of the SOL-GEL for the pre and post CMP curing approaches (Figure 2). It can be observed that longer CMP process times (2 x 40 s versus 1 x 60 s) result in a slightly lower roughness for both approaches. Moreover, the post-CMP curing wafers show higher root mean square (RMS) roughness values than the pre-CMP curing wafers. This result indicates a slight advantage of the pre-CMP curing compared to the post-CMP curing approach. However, the difference of all roughness results is very small, less than 0.3 nm. Moreover, all roughness results are below 0.6 nm.

3.2 Ellipsometry Porosimetry (EP)

Porosity and refractive index were measured by ellipsometric porosimetry (Figure 3). The SOL-GEL before curing (just with a soft bake at 150 °C) has a porosity of 4 % (SOL-GEL w/o cure). Before curing the presence of the acrylic polymer porogen will seal the SOL-GEL film almost completely. The very low porosity facilitates the chemical mechanical polishing of the SOL-GEL by protecting the material from CMP related damage. The SOL-GEL fully cured at 400 °C anneal temperature results in an OSG with 22 % porosity.

If the SOL-GEL is cured before CMP, the target porosity will not be reached. Only a porosity of 16 % is thereby obtained. However, if the CMP is executed before curing, the porosity is higher. Hence, a final porosity of 24 % can be obtained. In addition, if the pores are created at a later stage, the low-k material is protected from CMP influences (slurry, cleaning chemicals, etc.). Moreover, it has been shown that simply removing the moisture absorbed near the top interface by thermal desorption is not sufficient and must be accompanied by other physical methods to preserve TDDB lifetime [7, 8]. The moisture uptake during CMP will be less for the post-CMP curing approach. Furthermore the curing after CMP will help to remove any remaining moisture.

3.3 CMP Removal Rates (RR)

CMP tests were run on cured and uncured SOL-GEL blankets. Figure 4 shows the removal rates (RR) versus polish time.

For uncured wafers, a plateau on the RR curves is reached after approximately 60 s. In that case, a steady-state CMP process was established. Such warm up effects are often caused by increasing temperatures during the CMP process stabilizing after a certain time. After this initial test, the wafers were reused to determine the RR again. All wafers polished a second time (Run 2) showed a lower RR. This RR decrease is probably caused by a surface passivation of the SOL-GEL, likely introduced by the physical strain or a chemical interaction between surface and slurry/ cleaning chemistry.

For cured wafers, a lower RR rate is observed. The reason for the higher removal rates on non-cured wafers is probably the softness of the SOL-GEL. Wherein, the acrylic porogen has not been decomposed during the curing process and the material is less cross linked.

Next, the CMP process was transferred to patterned wafers. Profilometer measurements for erosion and dishing (Figure 5) and SEM cross-sections (Figure 6) were obtained from those wafers. In addition, profilometer scans across the dishing and erosion fields are shown after multiple runs. A reference structure (Figure 7) was chosen to calculate the SOL-GEL thickness removal above it (considering ~370 nm as thickness removal target). The profiler measurements and the SEM cross-sections were used to find out the CMP end-point. The process had to be adjusted until the erosion and dishing fields have similar values, indicating similar polishing above wider and narrower structures (different copper pattern density), and close to zero, ending in alignment with the SOL-GEL reference pad. Wafer #1 is an example of an over-polished wafer and the wafer #2 is an example of an under-polished wafer. Hence, the wafer #3 got an improved process. The obtained cross section SEM of the reference structure is depicted for each wafer in Figure 7. The SOL-GEL shrinkage is mainly an artifact induced by the electron beam of the SEM.

4. Summary

The feasibility of post-CMP integration of highly porous low-k materials has been demonstrated. This approach allows the integration of ULK materials that can be easily deposited by spin-on coating. The Cu lines remain protected by the CoWP cap and the barrier during RIE of the sacrificial dielectric and subsequent spin-on coating [5]. The post-CMP ULK replacement opens opportunities for the integration of ULK materials with extreme porosity and pore sizes that cannot be integrated with conventional schemes. This concept is therefore also a promising alternative to the air-gap integration. The removal rate of the non-cured SOL-GEL is sufficiently high for an acceptable throughput of the CMP process. Materials with low shrinkage must be used for pre-CMP curing. However, for the post-CMP curing approach the SOL-GEL overburden will be removed, reducing the shrinkage related stress components. Further studies need to proof manufacturability and reliability of the post-CMP integration of ULK.

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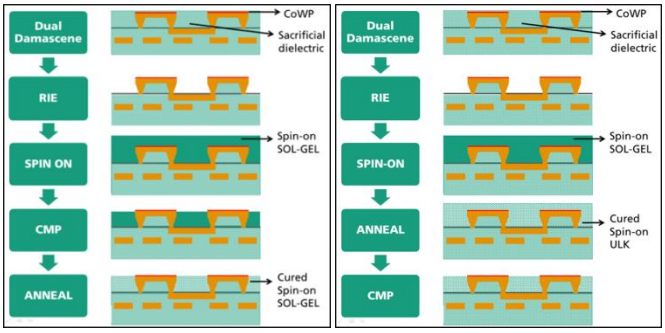

Figure 1. Overview of the post-CMP curing (left) and pre-CMP curing (right) in an extended Dual Damascene approach.

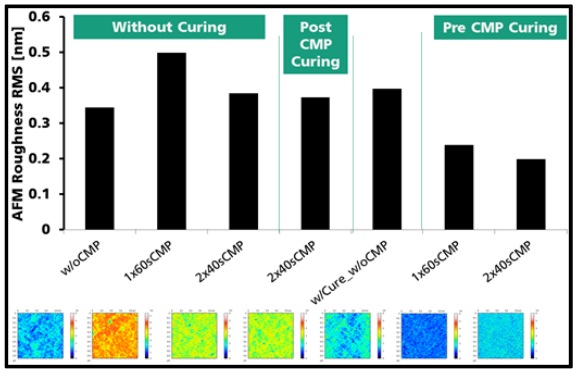

Figure 2. RMS roughness of pre-/ post-CMP cured SOL-GEL blanket wafers.

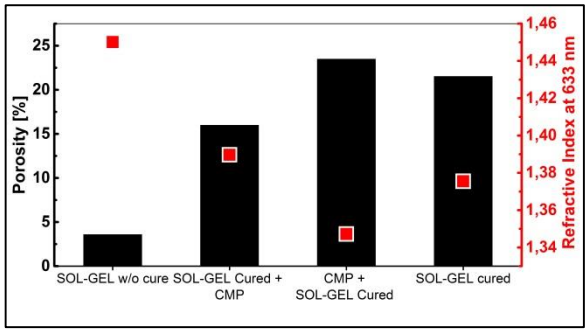

Figure 3. Porosity and refractive index.

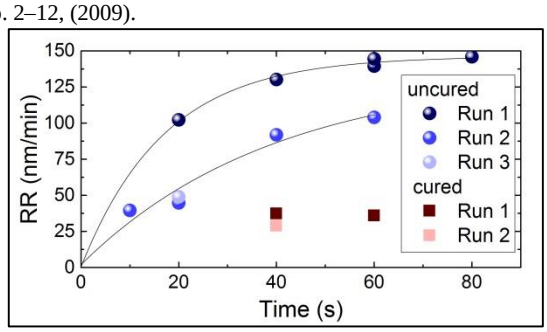

Figure 4. Removal Rate of SOL-GEL with and without curing versus CMP processing time.

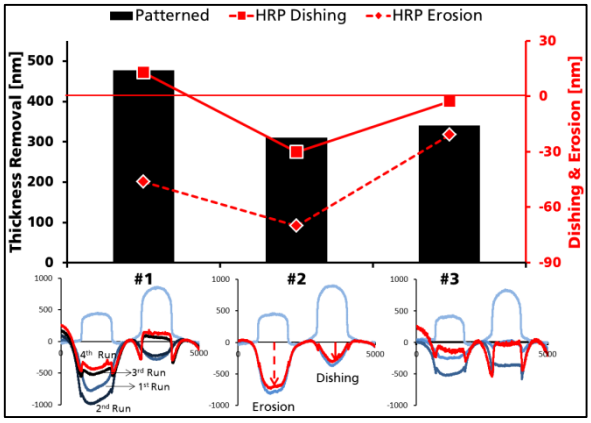

Figure 5. CMP Thickness Removal on patterned wafers with Dishing and Erosion.

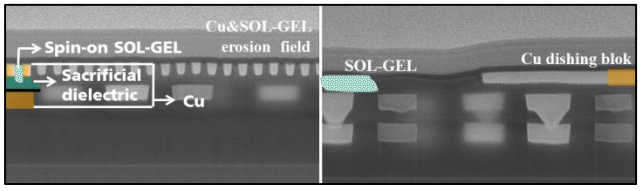

Figure 6. Erosion and Dishing fields from wafer #3.

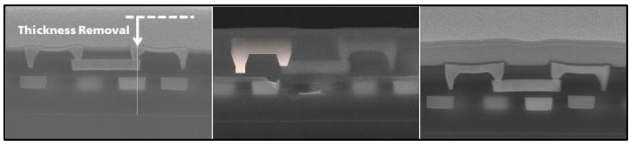

Figure 7. Reference structure of wafer #1 over-polished, #2 under-polished and #3 adjusted process.